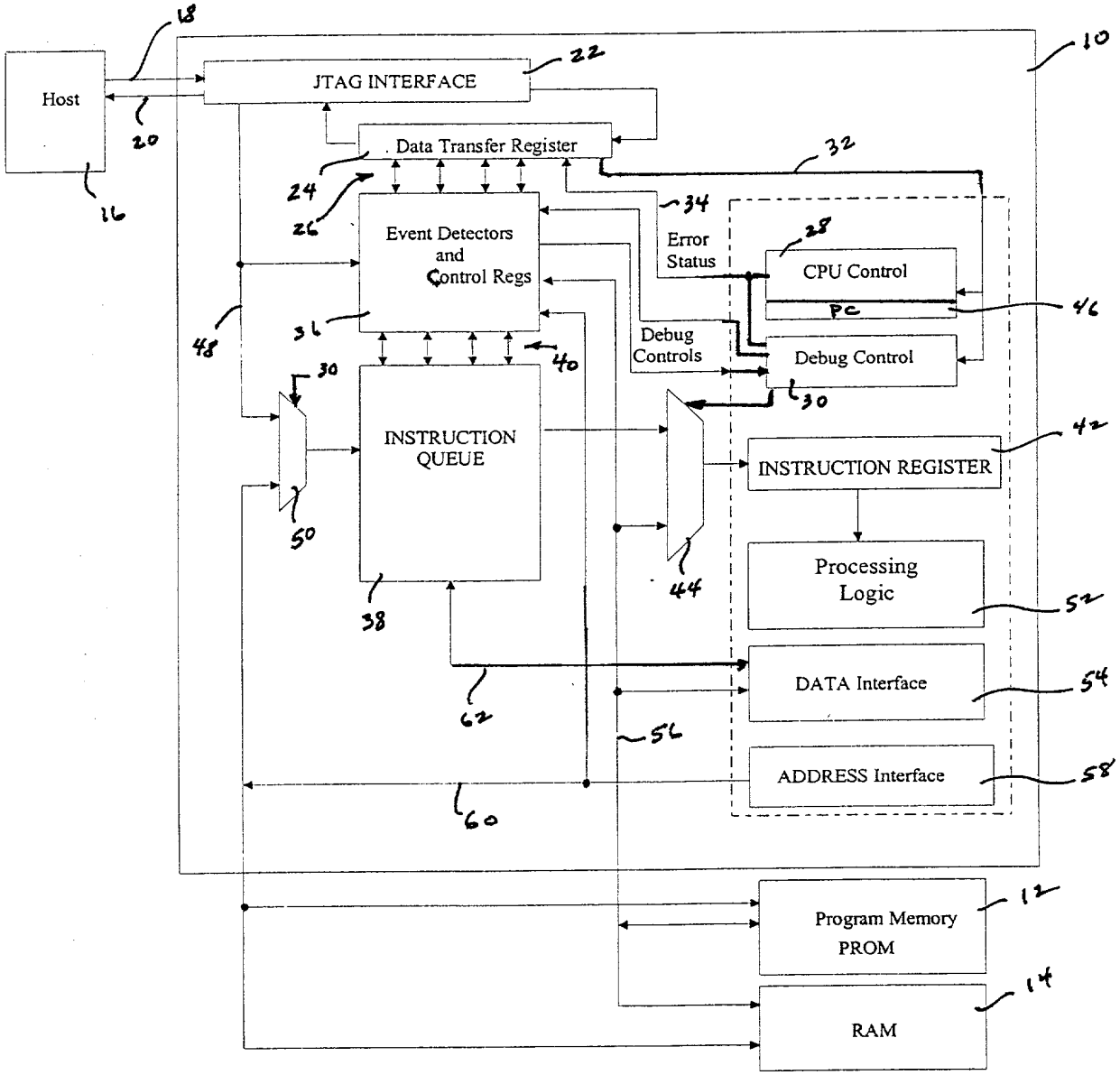
Host
JTAG INTERFACE
Data Transfer Register
Event Detectors and Control Regs
Error Status
CPU Control
PC
Debug Controls
Debug Control
INSTRUCTION QUEUE
INSTRUCTION REGISTER
Processing Logic
DATA Interface
ADDRESS Interface
Program Memory PROM
RAM
10
12
14
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
52
54
56
58
60
62

FIG. 1

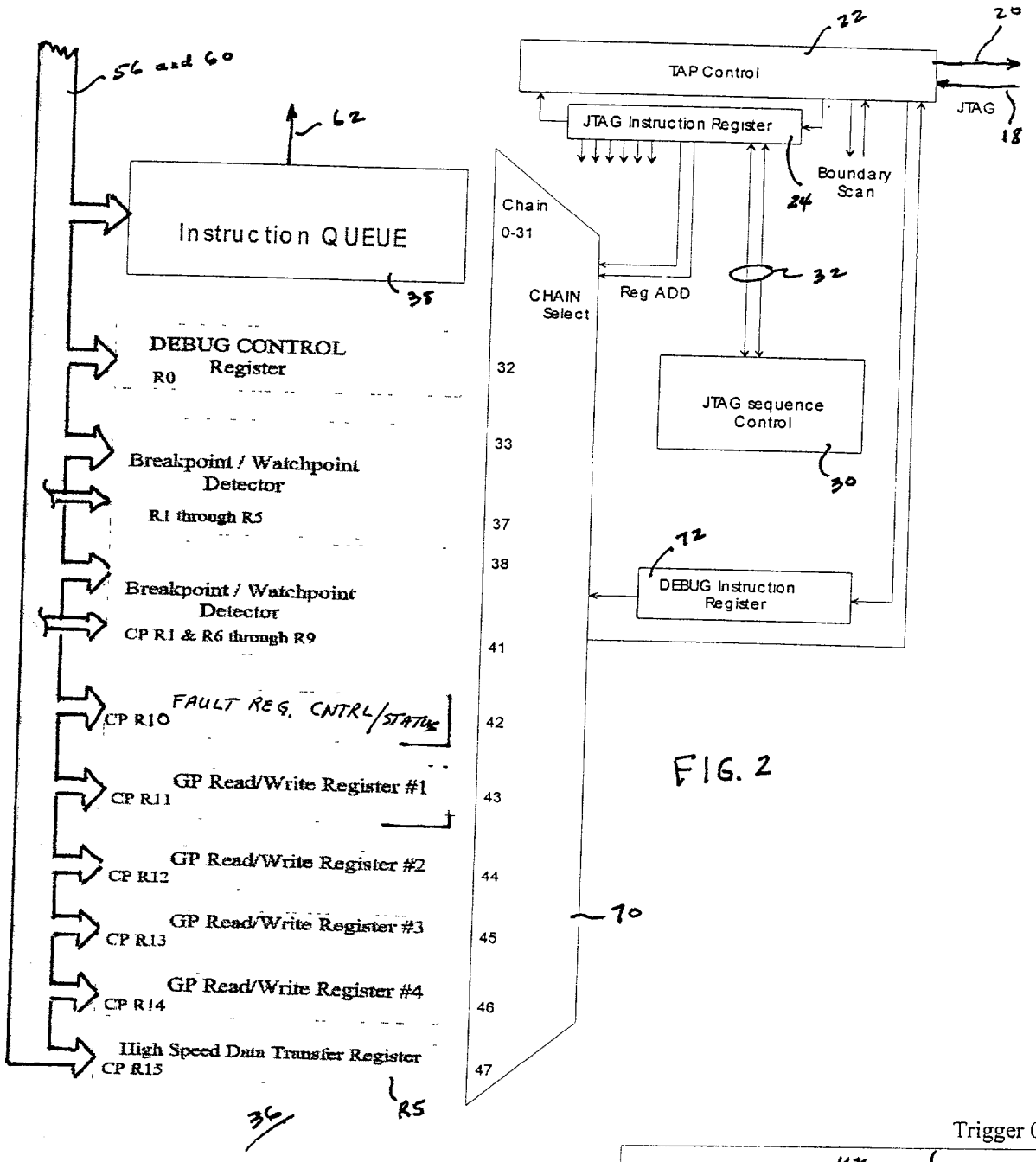
56 and 60
62
Instruction QUEUE
35
DEBUG CONTROL Register
R0
Breakpoint / Watchpoint Detector
R1 through R5
Breakpoint / Watchpoint Detector
CP R1 & R6 through R9
CP R10
FAULT REG. CNTRL/STATUS
CP R11
GP Read/Write Register #1
CP R12
GP Read/Write Register #2
CP R13
GP Read/Write Register #3
CP R14
GP Read/Write Register #4
CP R15
High Speed Data Transfer Register
R5
36
TAP Control
22
20
JTAG
18
JTAG Instruction Register
Boundary Scan
24
Chain 0-31
CHAIN Select
Reg ADD
32
JTAG sequence Control
30
DEBUG Instruction Register
72
32
33
37
38
41
42
43
44
45
46
47
70

FIG. 2

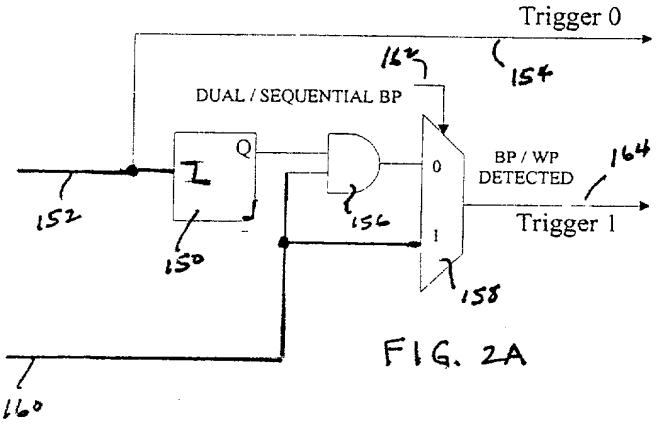
Trigger 0
162
154
DUAL / SEQUENTIAL BP
Q
D
0
1
BP / WP DETECTED
164
Trigger 1
152
150
156
158
160

FIG. 2A

Host Interface Mode Dependency Table				
Host Interface	JTAG		Peripherial	NONE
Debug Mode	External Monitor	Internal Monitor	Internal Monitor	Normal Operation
Debug Control Register	R/W via JTAG RD via CPU CPU WR enable via JTAG	R/W via JTAG & CPU	R/W via CPU	R/W via CPU
Break/Watch Points	Both BP & WP R/W via JTAG RD via CPU CPU WR enable via JTAG	WP Only R/W via JTAG & CPU	WP Only R/W via CPU	WP Only R/W via CPU
Communication Registers	R/W via JTAG RD via CPU	R/W via JTAG & CPU	R/W via CPU	R/W via CPU
Instruction Queue	Initiated via JTAG Debug IR R/W via JTAG RD via CPU	Initiated via CP14R0b24 R/W via JTAG & CPU	Initiated via CP14R0b24 R/W via CPU	Initiated via CP14R0b24 R/W via CPU

FIG. 3

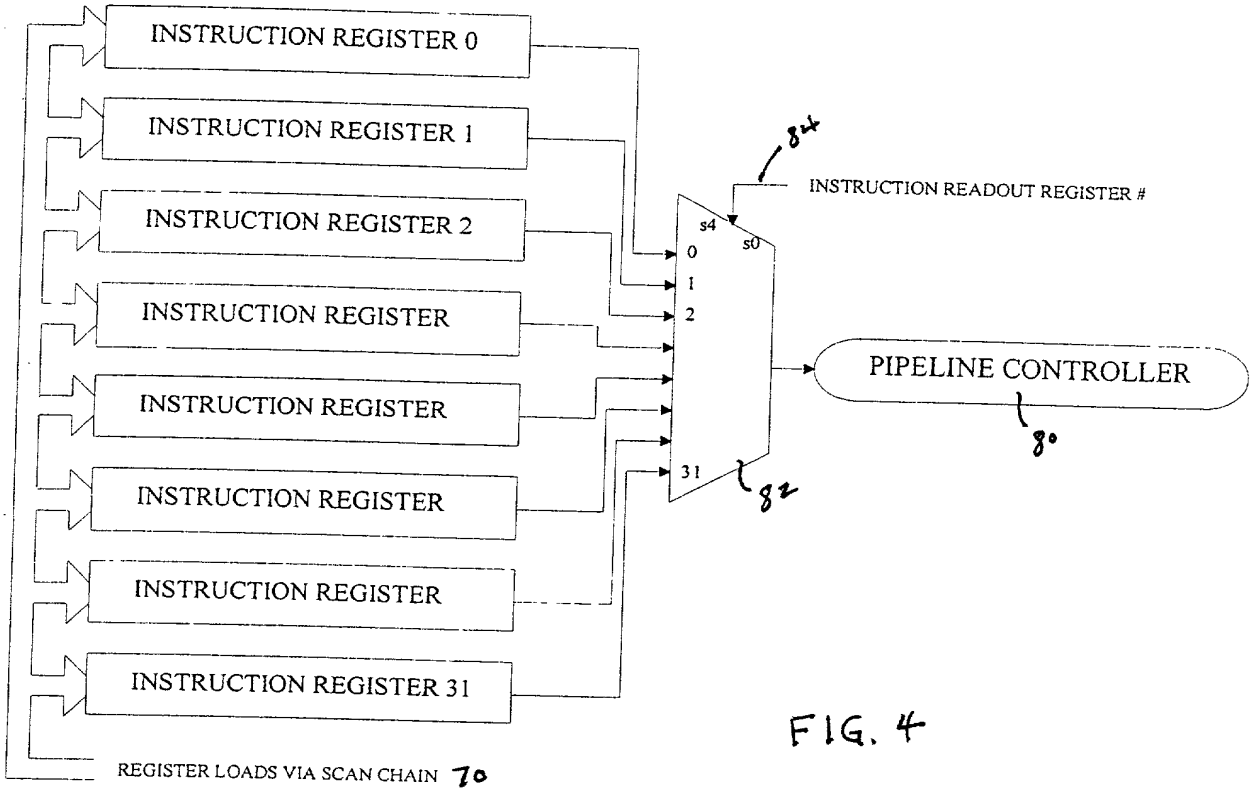
INSTRUCTION REGISTER 0
INSTRUCTION REGISTER 1
INSTRUCTION REGISTER 2
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER
INSTRUCTION REGISTER 31
REGISTER LOADS VIA SCAN CHAIN 70
84
INSTRUCTION READOUT REGISTER #
s4
s0
0
1
2
31
82
PIPELINE CONTROLLER
80

FIG. 4

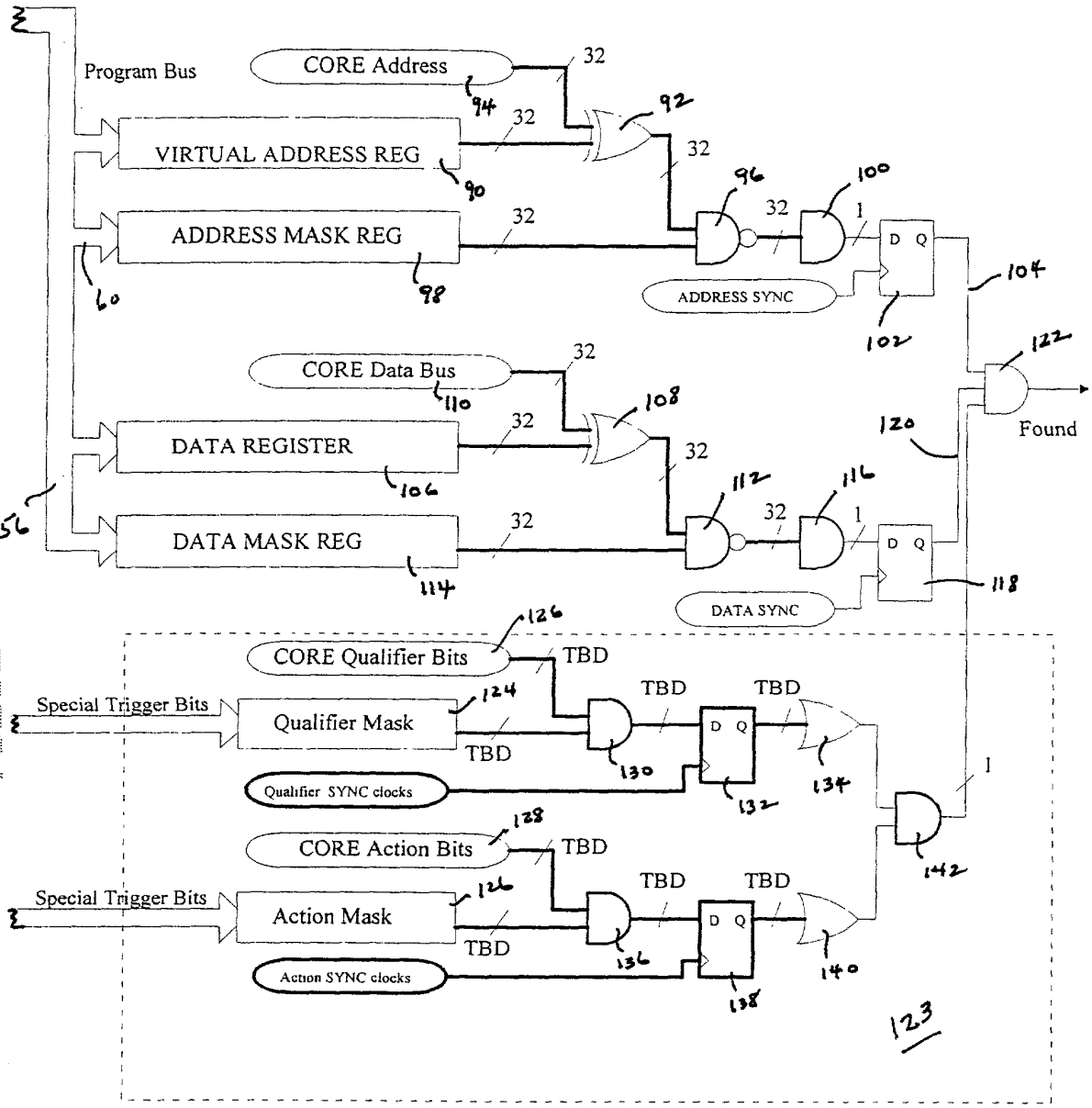
Program Bus
CORE Address
94
32
92
VIRTUAL ADDRESS REG
90
32
32
96
100
ADDRESS MASK REG
98
32
32
1
D Q
60
ADDRESS SYNC
102
104
CORE Data Bus
110
32
108
122
DATA REGISTER
106
32
32
120
Found
112
116
56
DATA MASK REG
114
32
32
1
D Q
118
DATA SYNC
126
CORE Qualifier Bits
TBD
Special Trigger Bits
124
Qualifier Mask
TBD
TBD
TBD
D Q
130
134
Qualifier SYNC clocks
132
I
128
CORE Action Bits
TBD
142
Special Trigger Bits
Action Mask
126
TBD
TBD
TBD
D Q
136
140
Action SYNC clocks
138
123

FIG. 5

MODE Access	MSB	Debug Control Register (register 0)																												LSB
R, W, RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG Debug	Read							R	R	R	R		R	R	R	R	R	R	R	R	R	WR	WR	R	R	WR	WR	R	R	R	R	R
JTAG ROM DEBUG	Write / Read Clear after read							WR	WR	R	R		RC	RC	RC	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	R	WR	WR
ROM DEBUG	Write / Read Clear after read							WR	WR	R	R		RC	RC	RC	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	WR	R	WR	WR
Reset	0							0	0	0			0			0	0	0	0	0	0	0	0	0	0	0	0	0		0	0
Definition	Count value (N)							Debug Instruction	Delay N	Instruction	Debug Entry Reason		Sequence	Detector 1	Detector 0	Debug EDAC	Debug Halt	Debug Halt	Debug Halt	Sequence	Sequence	Manual Trig	Detector 1	Enable	Detector 1	Manual Trig	Detector 0	Enable	Detector 0	JTAG	Enable Debug	Enable Debug

FIG. 6

MODE Access	MSB	IQ Fault Status/Control (register 10)																LSB
R,W,RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JTAG Debug	R	R	R	R	R	R	R	R	R	R	R	R	WR	WR	WR	WR	R	R	R	R	R	R	R	WR	R	R	R	R	R	R	R	R
JTAG ROM DEBUG													WR	WR	WR	WR							WR	WR	WR	WR			WR	WR	WR	WR
ROM DEBUG													WR	WR	WR	WR							WR	WR	WR	WR			WR	WR	WR	WR
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					FAULTS FOUND WITH IQ-EXE																				IQ Fault Control Bits							
Definition					Last FPU Fault	Last Data Abort							Did Not Execute IQ	FPU Fault during IQ	Data Abort during IQ								Read/Write Storage	Read/Write Storage	**Halt on Fault at end**	**Synchronize before**					Do not execute if	Do not execute if	

FIG. 7

Register		User Mode			
		JTAG DEBUG ENABLED JTAG Debug Mode (Bit 1 = 1) of the Debug Instruction Register.		JTAG DEBUG DISABLED JTAG Debug Mode (Bit 1 = 0) of the Debug Instruction Register.	
Name	Number	Read Access	Write Access	Read Access	Write Access
Debug Control	0	Read Allowed	Undefined Instr Treat as NOP	Read Allowed	Write Allowed to Upper byte
Others	1-15	Undefined Instr Return Debug Control	Undefined Instr Treat as NOP	Undefined Instr Return Debug Control	Undefined Instr Treat as NOP

FIG. 8

	MSB	Debug Instruction Register					LSB
	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	1
Definition	JTAG installed	Execute Instruction Queue	Single Step	Enable Interrupts in Debug	WDT Debug hold	JTAG Debug Mode	Run CPU

FIG. 11

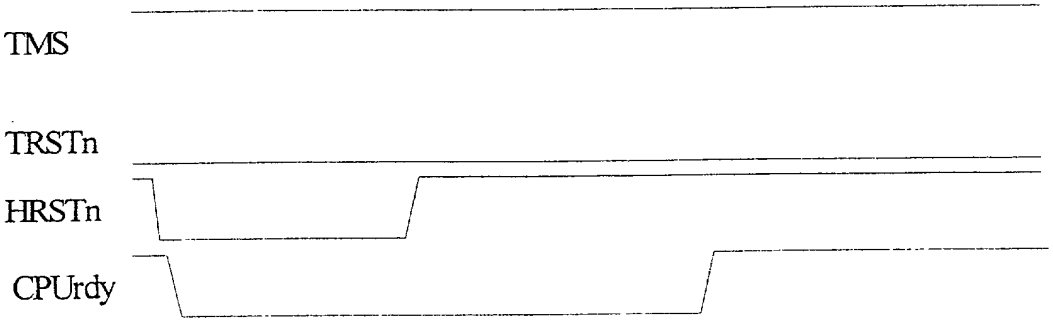

FIG. 9A

FIG. 9B

FIG. 9C

FIG. 9D

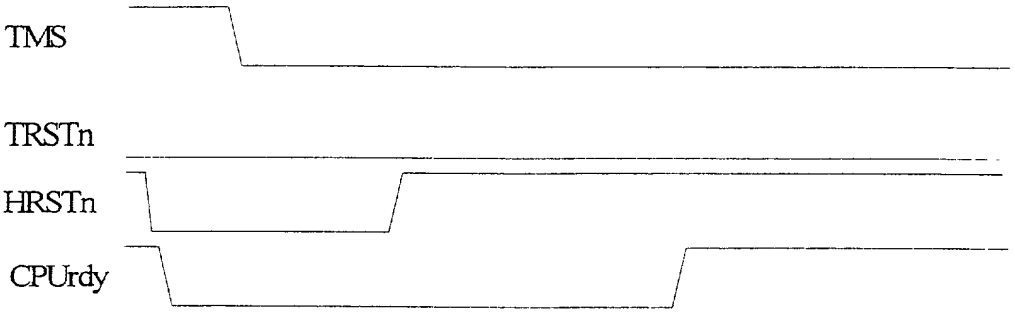

FIG. 10A

FIG. 10B

FIG. 10C

FIG. 10D

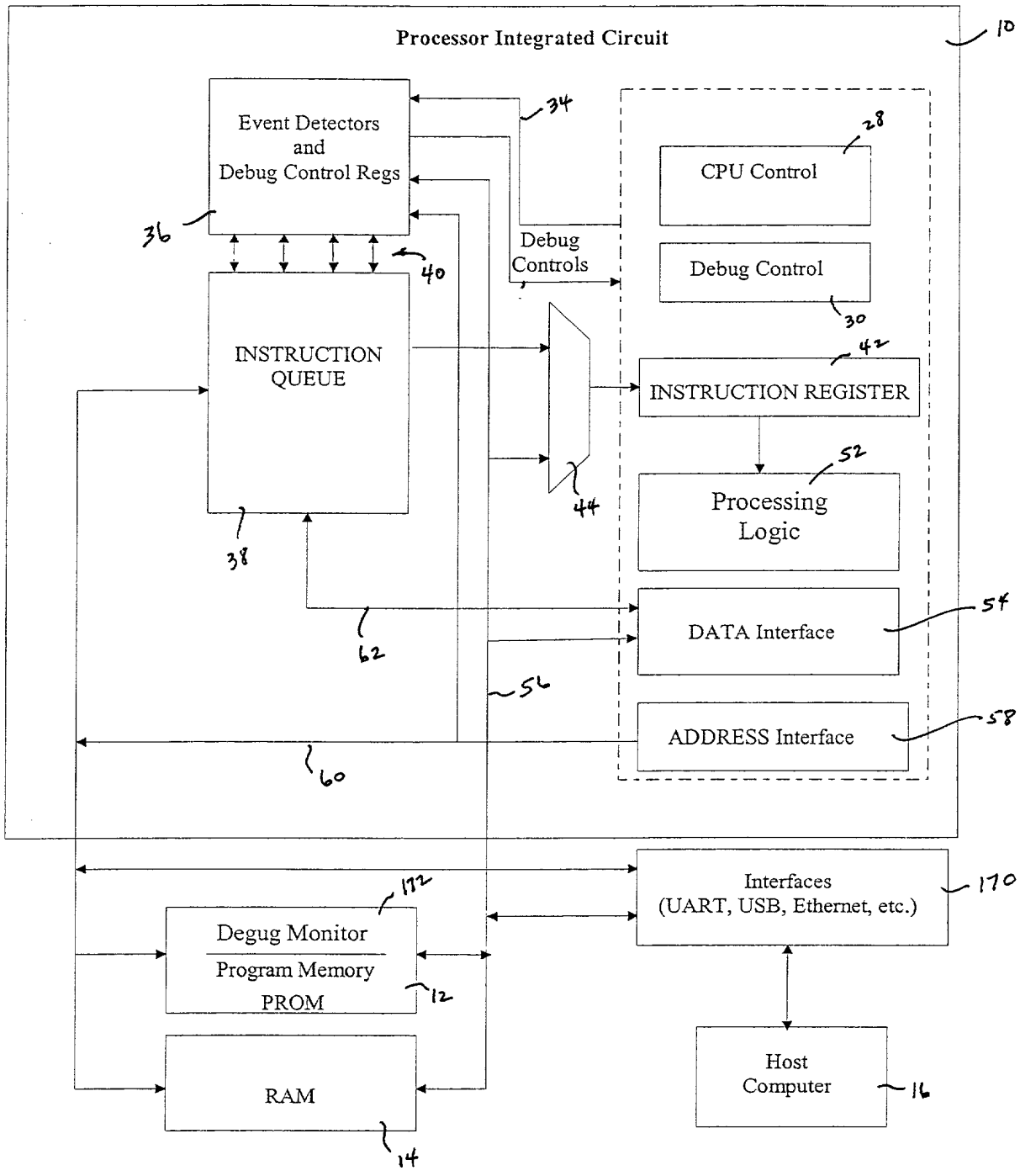
Processor Integrated Circuit
10
Event Detectors and Debug Control Regs
34
36
40
Debug Controls
CPU Control
28
Debug Control
30
INSTRUCTION QUEUE
42
INSTRUCTION REGISTER
44
52
Processing Logic
38
62
DATA Interface
54
56
ADDRESS Interface
58
60
Interfaces (UART, USB, Ethernet, etc.)
170
172
Degug Monitor
Program Memory
PROM
12
RAM
14
Host Computer
16

FIG. 12